

PATENT ABSTRACTS OF JAPAN

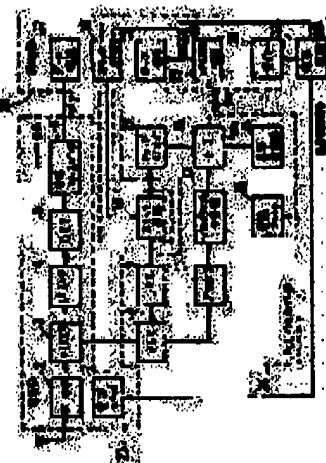
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H03L 7/10
H04B 1/26(21) Application number : **62-198480**(71) Applicant : **SHARP CORP**(22) Date of filing : **07.08.1987**(72) Inventor : **SUMIKAWA KEIICHIRO****(54) PHASE LOCKED LOOP CIRCUIT****(57) Abstract:**

PURPOSE: To reduce the lock time at intermittent operation by providing a switching means and a voltage storage means storing an input voltage to a voltage controlled oscillator circuit just before the open circuit between a phase comparator and an LPF.

CONSTITUTION: The switching circuit 16 interposed between the phase comparator (PD) 13 and the LPF 9, a charge pump 10 storing an input voltage to the voltage controlled oscillator circuit (VCO) 8 just before the open circuit and a switch control means 18 opening a loop by the switch 16 in the presence of the open circuit command, giving the said storage voltage to the VCO 8 when the open command exists and closing the loop by the switch 16 when the phase difference detected by the PD 13 reaches a prescribed value or below, are provided. When the power of the PLL circuit is switched from OFF to ON in the intermittent operation, the preceding frequency is taken over. Moreover, the loop is closed with a large phase difference and the frequency is not largely deviated. The lock time at the intermittent operation is shortened by the operation.

**LEGAL STATUS**

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⑩ 発明の名称 フェーズ・ロッド・ループ回路

⑪ 申 請 昭62-199460

⑫ 出 願 昭62(1987)8月7日

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3. 説明書

1. 発明の名称

フェーズ・ロッド・ループ回路

2. 本発明と特許の範囲

1. 位相比較回路と、ローパスフィルタと、電気制御物語回路とがループを形成して成るフェーズ・ロッド・ループ回路において、

位相比較回路とローパスフィルタの間をたはローパスフィルタと電気制御回路の間に介在されてループをオープンする手段と、オープン手段の電圧調整手段への入力電圧を整定する電圧調整手段と、オープン手段があると前記スイッチ手段でループをオープンするときにフェーズ角や幅がなると前記電圧調整手段に人力し前記位相比較回路で位相差を逆山し位相差が所定量以下となつたときに前記スイッチ手段でループをクローズするスイッチ回路手段とを具備したことを特徴とするフェーズ・ロッド・ループ回路。

3. 説明書の各部題名とその意味

(構造上の用語分野)

本発明は、フェーズ・ロッド・ループ回路に關し、主に特徴とは、期灰動作させる場合に周波数引き込み操作を緩和できるようにしたフェーズ・ロッド・ループ回路に関する。

(記載の技術)

コードレス電話やページャ等の無線周波回路においては、電波の播送を防ぐために、受信すべき電波の電力があるまでは強灰動作を行なっている。

即ち、受信部系全体に電力を供給して電波を受信できる状態で待機する待機動作と、受信部系の部分以外は電力の供給をカットして電波を受信できないが電力消費を抑制する休止動作とを交互に繰り返すことを行なっている。

フェーズ・ロッド・ループ回路（以下、PLR回路といふ）は、長手方向複数個のチューナ部のシンセサイザとして高く使われており、上述強灰動作時にば、アレシ西波も駆動動作をさせられている。

特開昭64-41522(2)

(発明が特許しようとする範囲)

ショーナ部にP.L.S.回路を用いた場合、アレシ回路の開放駆動を送る過程（ブルインレンジ）各種ロックされるまでも時間（ロッカタイム）は速い発電装置に入れない。従って、ロッカタイムは早い方が好ましい。

ところが、P.L.S.回路を間欠動作させると、その初期電圧オフから立ち上がるたる、初期ロックタイムが長くなってしまう問題点がある。

そこで、本発明の目的とするところは、間欠動作時にかかるロッカタイムを抑制可能としたP.L.S.回路を提供することにある。

(問題点を解決するための手段)

半導体のP.L.S.回路は、位相比較回路と、リバースフィルタと、電圧制御回路回路とがループを形成して成るフェード・ロッカ・ループ回路において、位相比較回路とリバースフィルタの間に介在したリバースフィルタと電圧制御回路の間に介在されてループをカットする手段と、オーバン電流の電圧制御回路への入力電圧を調整する電

圧記憶手段と、ゲート信号があると前記スイッチ手段でループをオープンすると共に、ローズ信号があると前記電圧制御回路回路に入力し前記位相比較回路で起動を検出し該回路が锁定状態となったらときに前記スイッチ手段でループをクローズするスイッチ記憶手段とを具備したことを特徴上の特徴とするものである。

【作用】

本発明のP.L.S.回路では、電圧記憶手段によつて電圧制御回路回路へ入力電圧を隔離してみるとことが出来るので、間欠動作時において、アレシ回路の電圧がオフからオンに切り替わった時、最初の電圧立ち上がりからスタートできる。従って、初期の初期ロック時間はそれを少なくて出来る。

また、スイッチ記憶手段によって、位相差が既定量以下になった時にループをクローズすることが出来るので、位相差が大きくなるループをクローズにして、初期ロックを大きく外してしまうことが防止される。

そこで、これらの作用より、間欠動作時にかけ

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るロッカタイムを短縮することが出来る。

そして、通常用断路器で開閉動作を伴う時の特有欠け時間とロックタイムの相違を持って短縮することが出来るようになるから、供給電力の一層低減できるようになる。

(実施例)

以下、図に示す実施例に基づいて本発明を更に詳しく説明する。ここに示す実施例は本発明の一実施例のP.L.S.回路を含む電源用開閉装置のブロック図、第1回は本発明にかかるスイッチ手段と電圧記憶手段とに対応する組合部分の具体的構成図、第2回は本発明にかかるスイッチ手段と電圧記憶手段とに対応する組合部分の具体構成図、第3回は第1回に示す組合部分の各部の符号説明図である。尚、図に示す実施例により本発明が規定されるものではない。

第1回に示す構成用開閉装置1は、受信部2と、P.L.S.レシーバセキイザー部3と、制御部4との3つの部分からなっている。

受信部2とは、送信公則の導線と同様であり、間欠動作のための電源スイッチ回路5が組合され

ている。

P.L.S.レシーバセキイザー部3とは、電圧制御回路6と、リバースフィルタ7と、チャージポンプ8と、アリストケーラ11と、アクダマップル分極器13と、電圧制御回路15と、監視用回路16とを有し、また、開欠動作のための電源スイッチ回路17を有している。

ここで注意すべきことは、リバースフィルタ7とチャージポンプ8との間に、スイッチ回路18が介在されていることである。

位相比較回路6とは、チャージポンプ8への出力の前に、位相差のあるときにパルスが由来するアンロック信号を由来している。

第2回は、リバースフィルタ7、スイッチ回路18、チャージポンプ8を具体的に割り出したものである。

制御部4とは、前記スイッチ回路17を制御するためのスイッチ制御回路19と、開欠動作を制御するためのタイマー回路21および電圧制御回路23と、前記位相比較回路6からのアン

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—129—

6

特開昭64-41522(3)

ク信号に応じて位相監視信号を出力するパルス発生回路20とを具備している。位相監視信号は、前記スイッチ回路11に入力されている。

第3回路は、スイッチ回路11、パルス発生回路20及び第4回路に示す信号読み取り部を參照し、前記動作時の動作を説明する。

まず、待ち受け動作の状態で、第3回路23、

アモルシングセラウザー回路24、制御回路25の全てに電力が供給され、電源を発電する状態で待機している。ここで説明用送信機1は、送信用半導体の送信チャンネルと、受信用半導体の制御チャンネルとを有しているが、待ち受け動作では、制御チャンネルの電源を切っている。

待ち受け動作を解説時間開始すると、タイマー回路21及び電源制御回路22から出力される電源オフ信号が「1」になると、すると、第3回に示すようにスイッチ回路11がアーリー、第2回に示すようにローパスフィルタのコンデンサC1は直列の電源を絶続した状態となる。

する周波数となり、それは次の待ち受け動作をさせる周波数も正確な周波数である。即ち、立ち上がりに遅れる時間が短められる。

ところで、位相比較回路11に入力される定位制御発振回路10からの信号と第3回路23からの信号の位相差が大きいと、定位号の周波数が奇数してしまって、ループがクローズされた時に周波数が大きく外れてしまう危険がある。

しかし、スイッチ回路11は、位相監視信号を待ってから駆動されるため、かかる周波数は必ずは固定される。即ち、第3回に示すように定位によって、周波数も上がりにはスイッチ回路11が駆動しないようになる。そして、位相差が大きくなる時に出力されるアンロック信号が入力されていふ時は、スイッチ回路11を閉じないようにする。そして、電源が完全に立ち上がり、且つ、位相差がなくなってアンロック信号が入力されない時はスイッチ回路11が閉じられる。

そこで結果、周波数がはじき放し、且つ、位相差のない状態でループがクローズされるので、周

期回路23は、スイッチ回路11を介してした後、電源スイッチ回路11及び13を作動し、受信部23とドリレシシングセラウザー部24の電源を遮断する。また、制御部25のデータ監視回路12、ロック検出回路13、パルス発生回路20の電源を遮断する。かくして、電源の受電が出来ないが、消費電力を抑制した休止動作に移行する。

休止動作を新規時間開始すると、タイマー回路21及び電源制御回路22は、電源オフ信号を「0」にし、定位号23及びアモルシングセラウザー回路24の電源をオンとする。また、制御部25のデータ監視回路12、ロック検出回路13、パルス発生回路20の電源をオンにする。

しかし、スイッチ回路11は、電源オフ信号が「0」となっても、パルス発生回路20からの位相監視信号が入力されないかぎり、ループをターゲットにしない。

そこで、電圧制御発振回路10の初期の周波数は、ローパスフィルタR1に接続されていた電圧に対応

周波数外れを生じず、暗時間でアモルシング回路24をオフする。

かくして、PLL回路のロックタイムを短縮できるため、待ち受け動作の時間も縮減できるようになる。そこで、説明すべき電源の電圧があるまでの時間に説明用送信機1が消費する電力を低減できることとなる。

【実用の効用】

本発明によれば、位相比較回路と、ローパスフィルタと、電圧制御発振回路とがループを形成して成るスイッチ・ロックド・ループ回路において、位相比較回路とローパスフィルタの間またはローパスフィルタと電圧制御回路の間に分離されてもループをオーブンする手段と、オープン状態の電圧制御発振回路への入力電圧を記憶する電圧記憶手段と、オーブル指令があると前記スイッチ手段でループをオーブンすると共にクローズ指令があると前記記憶電圧を前記電圧制御発振回路に入力し位相比較回路で位相差を検出しあループが固定されとなつたときに前記スイッチ手段でループ

特開昭64-41522(4)

をクローズするスイッチ切替手段とそれをしたことを示すとするフェーズ・マッタ・ループ回路が掲載され、これにより周波数計を読みに要する時間なしでロックタイムを短縮できるようになる。

そこで、かかるフェーズ・マッタ・ループ回路を用いた測定装置において、周波数計を立ち待機するまでの待ち受け動作の時間短縮を可能としたり、低消費電力化を実現できる。

4. 図面及び技術資料

第1図は本発明の一実施例のプロセス構成を示す測定用装置のブロック図、第2図は本発明におけるスイッチ手段と電圧切替手段とに對応する回路部分の具体的構成図、第3図は本発明にかけたスイッチ切替手段に対応する回路部分の具体構成図、附1図は第3図に示す回路部分の各部の符号表である。

【符号の説明】

1 ～ 8 带用受信機

1.1

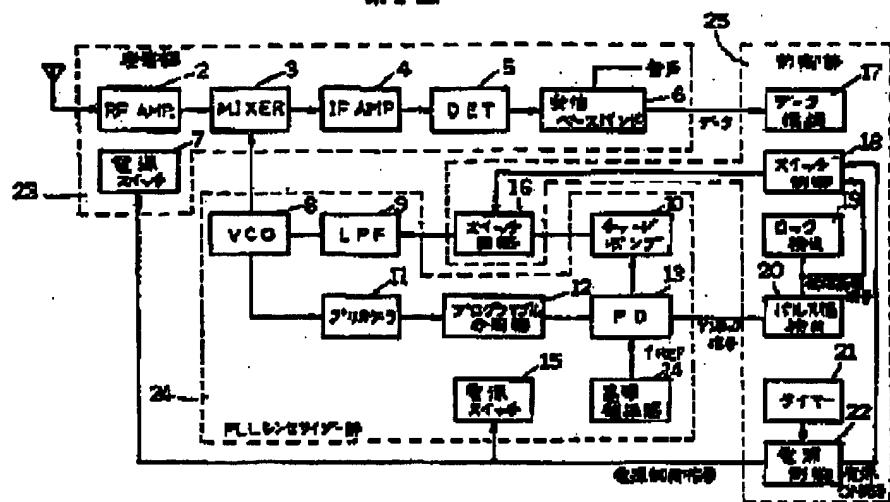
1.2

- 9 ～ 電気制御機器回路
- 10 ～ ワーパスフィルタ
- 11 ～ チューニングコントローラ
- 12 ～ 位相比較回路
- 13 ～ スイッチ回路
- 14 ～ スイッチ制御回路
- 20 ～ ベルヌル管回路
- 21 ～ フィマー回路
- 22 ～ 電磁制御回路
- 3.1 ～ 電源スイッチ回路

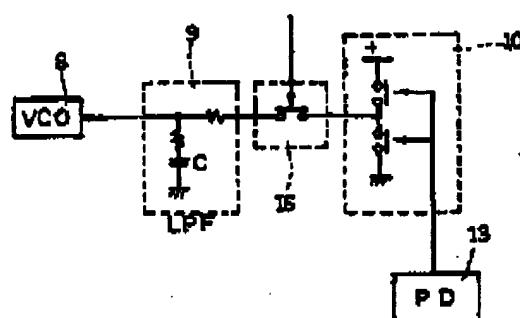
出願人 シャープ株式会社
代理人 特許士 本庄 実秀

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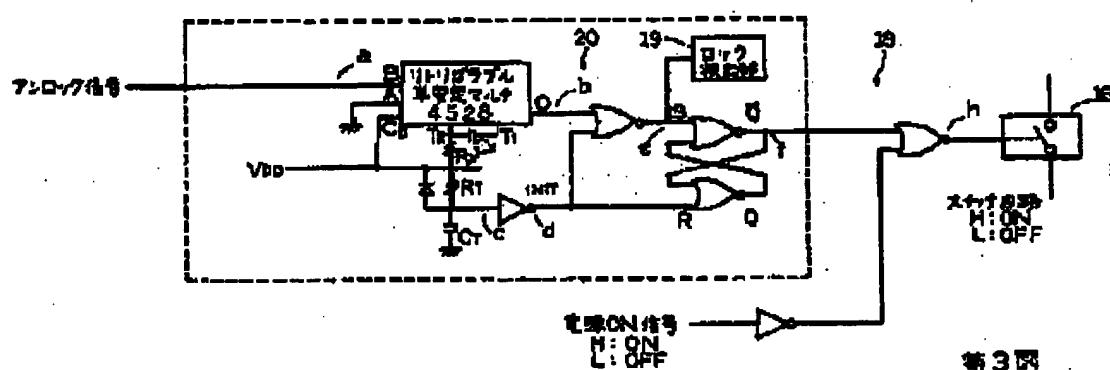
第1回



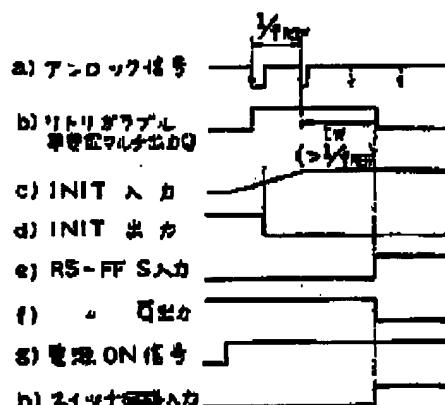
第2回



特許1284-41526(6)



第3回



第4回

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(71) Applicant : NEC CORP

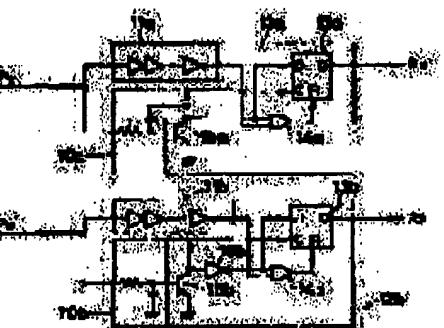
(22) Date of filing : 28.07.1993

(72) Inventor : JOKURA ATSUSHI

(54) PLL CIRCUIT**(57) Abstract:**

PURPOSE: To improve S/N of the PLL circuit in the frequency synthesizer of a reception system by providing a dead zone for phase comparison and realizing stable synchronous convergence.

CONSTITUTION: A phase leading PD pulse is delayed by a delay device 11b and is inputted to the clock input of a D-FF 13b. The PD pulse is integrated by a time constant circuit 10b, and this integral waveform is compared with the threshold of a transistor TR 15b, and, a pulse is generated when it is larger than this threshold. This pulse is inputted to the data input of the D-FF 13b to latch the PD pulse, and the D-FF 13b is reset by an OR gate 14b at the time of disappearance of the PD pulse. Its Q output RD is supplied to a charge pump and a loop filter to obtain the control voltage of a VCO. Consequently, the dead zone is determined by CR of the time constant circuit 10b and the threshold of the TR 15b, and the PD pulse larger than the dead zone is outputted as it is, and therefore, synchronous convergence is stabilized.

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CLAIMS

[Claim(s)]

[Claim 1] An armature-voltage control oscillation means and a phase-comparison means to make the phase comparison of this oscillation output frequency signal and external oscillation signalling frequency, It is a PLL circuit including a control-voltage generation means to generate the control voltage of the aforementioned armature-voltage control oscillation means according to this phase-comparison output, the aforementioned control-voltage generation means A delay means by which the aforementioned phase-comparison output is delayed, and the time constant circuit which considers the aforementioned phase-comparison output as an input, The PLL circuit characterized by being constituted including a latch means to cancel this latch state when the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears by the output of the aforementioned delay means so that the aforementioned control voltage may be generated using this latch output.

[Translation done.]

* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] Especially this invention relates to the PLL circuit used in order to obtain the stable synchronizing signal in strange recovery technology about a PLL (phase locked loop) circuit.

[0002]

[Description of the Prior Art] A PLL circuit detects the phase contrast of the reference frequency signal given from the outside, and the dividing output which carried out dividing of the oscillation output of VCO (voltage controlled oscillator), controls VCO by direct current voltage according to the phase contrast, and obtains a stable oscillation output.

[0003] In the receiving system, it mixed with the receiving RF signal by having made this oscillation output into the local oscillation signal, and the IF signal was created and alignment has been obtained for the frequency change at the time of a channel change by changing the division ratio of a counting-down circuit (program divider), or using a direct digital synthesizer etc. and changing the reference frequency signal itself to the source of a signal.

[0004] In local oscillation frequency synthesizer SASHIZA, for a high-speed frequency change, the high interest profit design of a system is performed, but on the other hand noise bandwidth becomes large, it is easy to incorporate noise in a system, and C/N-ary of an oscillation output pose a problem. The method of extending the neutral zone (DETTO zone) in a phase comparison as a negative measure in such a case is taken.

[0005] Drawing 5 is the circuit diagram showing the portion of the phase comparator of the conventional PLL circuit shown in JP,63-260317,A. reference frequency signal fR with which the 1st D-FF and 23 were impressed to the 2nd D-FF, and 24 was impressed [21] to the clocked-into terminal of 1st D-FF22 for a charge pump and 22 The 1st delayed delay circuit and dividing signal fP with which 25 was impressed to the clocked-into terminal of 2nd D-FF23 It is the 2nd delayed delay circuit. 25 and 24 are delay circuits and 28 and 29 are the DETTO zone expansion signal DZ. It is the circuit which responds and chooses the amount of delay.

[0006] Next, operation is explained. input terminal D1 of D-FF22 *** -- reversal output Q2 of D-FF it impresses -- having -- input terminal D2 of D-FF23 *** -- reversal output Q1 of D-FF22 it impresses -- having -- output Q1 it is impressed by the gate of NMOS26 of the charge pump circuit 21 -- having -- output Q2 It is impressed by the gate of NMOS27.

[0007] DETTO zone expansion signal DZ If it turns OFF ("0"), the delay signal of the last stage of a delay circuit will be chosen from selection circuitries 28 and 29.

[0008] First, dividing signal fP It receives and is the reference frequency signal fR. It is fP, as it is shown in drawing 6 (A), when the phase is in agreement. fR By the standup, both D-FF 22 and 23 incorporate a mutual reversal output "1", and it is an output Q1 respectively. And Q2 It outputs. These outputs Q1 and Q2 It goes up by the inclination shown as a solid line like drawing 6 (C), and is threshold voltage Vt. It is TD the time of reaching. Output R1 of selection circuitries 28 and 29 R2 It starts.

[0009] That is, the amount of the maximum delay of delay circuits 24 and 25 is TD. It has designed so that it may become equal, and it is an output R1 and R2. It is reset and both D-FF 22 and 23 are outputs Q1 and Q2. It falls, therefore neither of NMOSes 26 and 27 turn on in this case, and the output PD according to phase contrast is not outputted.

[0010] As shown by drawing 6 (B), after fR ' has become early for 10ns, D-FF22 incorporates "1" and is an output Q1. It starts like dotted-line ** of (C). It is behind for 10ns and D-FF23 is fP. "1" is incorporated in a standup and it is the output Q2. It goes up. Next, when R1 ' is outputted from a selection circuitry 28, it is reset and D-FF23 is an output Q2. Vt Before reaching, it falls like dashed line ** of (C).

[0011] On the other hand, it is the output Q1 of D-FF22. Vt It reaches and is the output R2 of a selection circuitry 29. D-FF22 will be reset. Therefore, output Q1 Vt The period which became above, and NMOS26 are turned on, and the output PD according to phase contrast "0" is outputted. That is, in the case of drawing 6 (C), it is fR. When it becomes early, it is an output R2. Before being outputted, it is surely Vt. Reaching, a dead zone serves as zero.

[0012] Next, DZ= "1" is a case and, as for drawing 6 (D), the delay signal with few amounts of delay than the time of DZ=

is TD. Since it becomes early, it is Q1. Q2 Vt D-FF 22 and 23 is reset without reaching.

[0013] Now and output R1 R2 TD It is fR when it is a delay signal early for 10ns. When it becomes early for 10ns like drawing 6 (D), it is the output Q1 of D-FF22. It goes up, as shown by the solid line of (D), and it is Vt. Since an output R2 occurs just before reaching, D-FF22 is reset, and it is Q1. It falls.

[0014] Therefore, in the case of drawing 6 (E), it is fR. fP Phase contrast is an output Q1 within in 10ns. Vt Output PD corresponding to [before reaching D-FF22 will surely be reset and NMOS26 is turned on, and] phase contrast It is not generated. That is, the dead zone for 10ns is prepared. the same -- fP if it comes out 10 or less ns when it becomes earlier than fR -- output Q2 of D-FF23 Vt Since D-FF23 is reset before reaching, the dead zone for 10ns occurs.

[0015] By preparing a dead zone, frequent generating of a control pulse which serves as disturbance of VCO in the state where the PLL circuit locks was prevented, and noise signals, such as a jitter nozzle, were also omitted, and S/N is improved sharply.

[0016]

[Problem(s) to be Solved by the Invention] In the PLL circuit constituted from a conventional phase-comparison circuit mentioned above, there is a problem on which the reaction of a system becomes slow to the phase contrast near the dead zone.

[0017] For example, fR fP When the case where received and it becomes early for 12ns is assumed, it comes to be shown in drawing 7. In the state of the dead zone 0 of DZ = "0", it is an output Q1. Vt It can put at about 12ns and the time it is over is PD. Although "1" is outputted for 12ns as a signal a dead-zone 10ns [of DZ = "1"] state -- output Q1 Vt about 2ns of time to exceed -- becoming -- PD As a signal, for 2ns continues but the rate of the integration voltage value change which controls VCO which lets a loop filter pass boils "1" dully.

[0018] If the property of this phase comparison is shown in drawing, it will become like drawing 8. fR fP Since the time which sees relatively and is deleted in 10ns for the dead-zone setup becomes small when phase contrast is large, although influence decreases, the sensitivity as a remarkable system deteriorates near the dead zone.

[0019] Specifically, although it is convenient to change to near shift frequency at the time of the change of the oscillation frequency of a PLL circuit, alignment near a convergence value is affected and there is a trouble which the phenomenon in which vibration drags on to a convergence value tends to produce.

[0020] The purpose of this invention is offering the PLL circuit which enabled stable synchronous convergence, preparing a dead zone at the time of a phase comparison.

[0021]

[Means for Solving the Problem] A phase-comparison means to make the phase comparison of an armature-voltage control oscillation means, and this oscillation output frequency signal and external oscillation signalling frequency according to this invention, It is a PLL circuit including a control-voltage generation means to generate the control voltage of the aforementioned armature-voltage control oscillation means according to this phase-comparison output. the aforementioned control-voltage generation means A delay means by which the aforementioned phase-comparison output is delayed, and the time constant circuit which considers the aforementioned phase-comparison output as an input, When the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears by the output of the aforementioned delay means, the PLL circuit characterized by being constituted including a latch means to cancel this latch state so that the aforementioned control voltage may be generated using this latch output is obtained.

[0022]

[Example] It explains in detail, referring to a drawing about the example of this invention below.

[0023] Drawing 1 is the block diagram of the example of this invention, and is reference frequency fR. The output of generated VCO 1 turns into one input of a phase comparator 3. Frequency fP which carried out dividing of the oscillation frequency of VCO7 to the other inputs of this phase comparator 3 with the counting-down circuit 2 The signal is impressed.

[0024] It is the lead signal PD of the pulse width according to the phase contrast from a phase comparator 3. It is behind, Signal PU is outputted and it is inputted into filter circuits 4a and 4b, respectively. These filter circuits 4a and 4b are circuits of the feature portion of this invention, and the one example is shown in drawing 2. They are PD and PU, a dead zone being set up in these filter circuits 4a and 4b. Phase contrast signals RU and RD with which pulse width (phase contrast information is included) does not change It is generated.

[0025] These phase contrast signals RU and RD It becomes the control voltage of VCO7 by being inputted into a loop filter 6 and finding the integral through the charge pump 5.

[0026] The output of this VCO7 serves as local oscillation frequency in a receiving system, change instructions of a receiving channel are answered, the oscillation frequency fR of reference frequency VCO 1 and the division ratio of the program divider 2 are controlled, and the PLL frequency synthesizer is constituted.

[0027] Drawing 2 (A) and (B) are each example circuit diagram of the filter circuits 4a and 4b of drawing 1. First, if

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drawing 2 (A) is referred to, it is the lead signal PU. It is inputted into respectively. The delay output of delay circuit 11a turns into a clocked into of D-FF13a which constitutes latch circuit 12a. [0028] The output of time constant circuit 10a turns into a base input of PNP transistor 15a which constitutes latch circuit 12a, and the emitter output of this transistor 15a turns into one input of OR-gate 14a while turning into a data input of D-FF13a. The delay output of delay circuit 11a is impressed to the other inputs of this OR-gate 14a, or the output is the reset input of D-FF13a. And the reversal Q output of D-FF13a is RU. It becomes.

[0029] Drawing 2 (B) is the delay signal PD. Although it consists of delay circuit 11b, time constant circuit 10b, and latch circuit 12b concretely also about the side The polarity of the power supply line of time constant circuit 10b and the polarity of transistor 15b in a latch circuit progress, and it is Signal PU. It has become contrary to a side. Moreover, the collector output of transistor 15b is inverted in inverter 16b, and is the data input of D-FF13b, and one input of OR-gate 14b.

[0030] Drawing 3 is each signal wave form view showing operation of the circuit of drawing 2 (B), and is fR, fP When it receives and a phase is overdue, it is the delay signal PD. Two PDs from which it is a thing at the time of being outputted, and it is behind in this example, and a degree differs The pulse is shown.

[0031] PD shown in (C) A pulse is changed into the loose wave (integration wave) of the standup shown in (d) with the time constant of time constant circuit 10b. This wave is the threshold Vt of transistor 15b. PD which is not attained By the pulse, transistor 15b does not turn on and, therefore, the data input signal (D input signal) from inverter 16b to D-FF13b is not generated. On the other hand, an integration wave is Threshold Vt. PD to attain By the pulse, transistor 15b is generated, as it turns on and a data input signal shows (e) from inverter 16b, and for this data input signal, an integration wave is Threshold Vt. It is generated until it becomes smallness.

[0032] the clocked into of D-FF13b -- PD a pulse -- time tD only -- **** delay PD shown in delayed (f) The pulse is supplied. Here, it is a time delay tD. Same [in the time tM (refer to drawing (e)) to become settled with the time constant of time constant circuit 10b / almost] or it is tM. tD If it selects to smallness a little, it synchronizes with the standup timing of a clock signal (delay pulse PD), and a data input signal is incorporated and latched to D-FF13b.

[0033] Delay PD It is the filter circuit output RD which a latch state is reset and is shown in (g) as a result since D-FF13b will be reset by the output of OR-gate 14b, if a pulse falls. It will be obtained.

[0034] Therefore, lead signal PD according to phase contrast Therefore, it is the threshold Vt of filter circuit 12b, without being inputted into the latter charge pump 5 by letting filter circuit 4b (drawing 1) pass depending on the degree of the phase contrast. Time tM to become settled It becomes a dead zone.

[0035] phase-lead-lag-network signal PD exceeding a dead zone ***** -- without the wave of the pulse changing, since there is no bird clapper dully like the former comparatively, the thing of the integration [by which it is outputted to the charge pump 5] voltage value change which controls [near the dead zone / come out and] VCO7 shown in drawing 4 as a phase-comparison property is obtained.

[0036] In addition, outputs RU and RD of filter circuits 4a and 4b PU and PD Receiving time delay TD If it attaches, it is a dead zone tM. It can compare and ignore at the convergence time (order for 1 or less ms) demanded also as 100ns (10MHZ) or more than it at the time of the channel change of local oscillation frequency.

[0037] Stopping at the circuit of drawing 2 only being shown in an example, it is clear for various circuit deformation to be possible.

[0038]

[Effect of the Invention] There is an effect that a highly efficient PLL circuit without vibration near the convergence value or a tailing phenomenon is realizable, at the time of a channel change, setting up the dead zone in a phase comparison, when PLL is designed by high interest profit for the high-speed channel change which was described above and which is demanded in a PLL receiving system like according to this invention.

[0039] If it states quantitatively, there is an improvement of 10dB or more with an S/N value, and shortening for 2ms or more can be aimed at in channel change convergence time.

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TECHNICAL FIELD

[Industrial Application] Especially this invention relates to the PLL circuit used in order to obtain the stable synchronizing signal in strange recovery technology about a PLL (phase locked loop) circuit.

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PRIOR ART

[Description of the Prior Art] A PLL circuit detects the phase contrast of the reference frequency signal given from the outside, and the dividing output which carried out dividing of the oscillation output of VCO (voltage controlled oscillator), controls VCO by direct current voltage according to the phase contrast, and obtains a stable oscillation output.

[0003] In the receiving system, it mixed with the receiving RF signal by having made this oscillation output into the local oscillation signal, and the IF signal was created and alignment has been obtained for the frequency change at the time of a channel change by changing the division ratio of a counting-down circuit (program divider), or using a direct digital synthesizer etc. and changing the reference frequency signal itself to the source of a signal.

[0004] In local oscillation frequency synthesizer SASHIZA, for a high-speed frequency change, the high interest profit design of a system is performed, but on the other hand noise bandwidth becomes large, it is easy to incorporate noise in a system, and C/N-ary of an oscillation output pose a problem. The method of extending the neutral zone (DETTO zone) in a phase comparison as a negative measure in such a case is taken.

[0005] For a charge pump and 22, 21 is the reference frequency signal fR with which drawing 5 was the circuit diagram showing the portion of the phase comparator of the conventional PLL circuit shown in JP,63-260317,A, the 1st D-FF and 23 were impressed to the 2nd D-FF, and 24 was impressed to the clocked-into terminal of 1st D-FF22. 25 is the 1st delayed delay circuit and the dividing signal fP impressed to the clocked-into terminal of 2nd D-FF23. It is the 2nd delayed delay circuit. 25 and 24 are delay circuits and 28 and 29 are the DETTO zone expansion signal DZ. It is the circuit which responds and chooses the amount of delay.

[0006] Next, operation is explained. input terminal D1 of D-FF22 **** -- reversal output Q2 of D-FF it impresses -- having -- input terminal D2 of D-FF23 **** -- reversal output Q1 of D-FF22 it impresses -- having -- output Q1 it is impressed by the gate of NMOS26 of the charge pump circuit 21 -- having -- output Q2 It is impressed by the gate of NMOS27.

[0007] DETTO zone expansion signal DZ If it turns OFF ("0"), the delay signal of the last stage of a delay circuit will be chosen from selection circuitries 28 and 29.

[0008] First, dividing signal fP It receives and is the reference frequency signal fR. It is fP, as it is shown in drawing 6 (A), when the phase is in agreement. fR By the standup, both D-FF 22 and 23 incorporate a mutual reversal output "1", and it is an output Q1 respectively. And Q2 It outputs. These outputs Q1 and Q2 It goes up by the inclination shown as a solid line like drawing 6 (C), and is threshold voltage Vt. It is TD the time of reaching. Output R1 of selection circuitries 28 and 29 R2 It starts.

[0009] That is, the amount of the maximum delay of delay circuits 24 and 25 is TD. It has designed so that it may become equal, and it is an output R1 and R2. It is reset and both D-FF 22 and 23 are outputs Q1 and Q2. It falls, therefore neither of NMOSes 26 and 27 turn on in this case, and the output PD according to phase contrast is not outputted.

[0010] As shown by drawing 6 (B), after fR ' has become early for 10ns, D-FF22 incorporates "1" and is an output Q1. It starts like dotted-line ** of (C). It is behind for 10ns and D-FF23 is fP. "1" is incorporated in a standup and it is the output Q2. It goes up. Next, when R1 ' is outputted from a selection circuitry 28, it is reset and D-FF23 is an output Q2. Vt Before reaching, it falls like dashed line ** of (C).

[0011] On the other hand, it is the output Q1 of D-FF22. Vt It reaches and is the output R2 of a selection circuitry 29. D-FF22 will be reset. Therefore, output Q1 Vt The period which became above, and NMOS26 are turned on, and the output PD according to phase contrast "0" is outputted. That is, in the case of drawing 6 (C), it is fR. When it becomes early, it is an output R2. Before being outputted, it is surely Vt. Reaching, a dead zone serves as zero.

[0012] Next, DZ= "1" is a case and, as for drawing 6 (D), the delay signal with few amounts of delay than the time of DZ= "0" is chosen. It is f R first. fP When the phase is in agreement, it is the output R1 of a delay circuit. R2 What is generated is TD. Since it becomes early, it is Q1. Q2 Vt D-FF 22 and 23 is reset without reaching.

[0013] Now and output R1 R2 TD It is fR when it is a delay signal early for 10ns. When it becomes early for 10ns like drawing 6 (D), it is the output Q1 of D-FF22. It goes up, as shown by the solid line of (D), and it is Vt. Since an output R2 occurs just before reaching, D-FF22 is reset, and it is Q1. It falls.

[0014] Therefore, in the case of drawing 6 (E), it is fR. fP Phase control corresponding to [before reaching D-FF22 will surely be reset and NMOS26 is turned on, and] phase contrast It is not generated. That is, the dead zone for 10ns is prepared. the same – fP if it comes out 10 or less ns when it becomes earlier than fR – output Q2 of D-FF23 Vt Since D-FF23 is reset before reaching, the dead zone for 10ns occurs.

[0015] By preparing a dead zone, frequent generating of a control pulse which serves as disturbance of VCO in the state where the PLL circuit locks was prevented, and noise signals, such as a jitter nozzle, were also omitted, and S/N is improved sharply.

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EFFECT OF THE INVENTION

[Effect of the Invention] There is an effect that a highly efficient PLL circuit without vibration near the convergence value or a tailing phenomenon is realizable, at the time of a channel change, setting up the dead zone in a phase comparison, when PLL is designed by high interest profit for the high-speed channel change which was described above and which is demanded in a PLL receiving system like according to this invention.

[0039] If it states quantitatively, there is an improvement of 10dB or more with an S/N value, and shortening for 2ms or more can be aimed at in channel change convergence time.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the PLL circuit constituted from a conventional phase-comparison circuit mentioned above, there is a problem on which the reaction of a system becomes slow to the phase contrast near the dead zone.

[0017] For example, fR fP When the case where received and it becomes early for 12ns is assumed, it comes to be shown in drawing 7. In the state of the dead zone 0 of DZ = "0", it is an output Q1. Vt It can put at about 12ns and the time it is over is PD. Although "1" is outputted for 12ns as a signal a dead-zone 10ns [of DZ = "1"] state – output Q1 Vt about 2ns of time to exceed -- becoming -- PD As a signal, for 2ns continues but the rate of the integration voltage value change which controls VCO which lets a loop filter pass boils "1" dully.

[0018] If the property of this phase comparison is shown in drawing, it will become like drawing 8 . fR fP Since the time which sees relatively and is deleted in 10ns for the dead-zone setup becomes small when phase contrast is large, although influence decreases, the sensitivity as a remarkable system deteriorates near the dead zone.

[0019] Specifically, although it is convenient to change to near shift frequency at the time of the change of the oscillation frequency of a PLL circuit, alignment near a convergence value is affected and there is a trouble which the phenomenon in which vibration drags on to a convergence value tends to produce.

[0020] The purpose of this invention is offering the PLL circuit which enabled stable synchronous convergence, preparing a dead zone at the time of a phase comparison.

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MEANS

[Means for Solving the Problem] They are the time constant circuit which is the PLL circuit which includes an armature-voltage-control oscillation means, a phase-comparison means make the phase comparison of this oscillation output-frequency signal and external oscillation signalling frequency, and a control-voltage generation means generate the control voltage of the aforementioned armature-voltage-control oscillation means according to this phase-comparison output according to this invention, and the aforementioned control-voltage generation means carries out as an input in a delay means to by which the aforementioned phase-comparison output is delayed, and the aforementioned phase-comparison output, and the output of the aforementioned delay means. When the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears, the PLL circuit characterized by being constituted including a latch means to cancel this latch state so that the aforementioned control voltage may be generated using this latch output is obtained.

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EXAMPLE

[Example] It explains in detail, referring to a drawing about the example of this invention below.

[0023] Drawing 1 is the block diagram of the example of this invention, and is reference frequency fR. The output of generated VCO 1 turns into one input of a phase comparator 3. Frequency fP which carried out dividing of the oscillation frequency of VCO7 to the other inputs of this phase comparator 3 with the counting-down circuit 2. The signal is impressed.

[0024] It is the lead signal PD of the pulse width according to the phase contrast from a phase comparator 3. It is behind. Signal PU is outputted and it is inputted into filter circuits 4a and 4b, respectively. These filter circuits 4a and 4b are circuits of the feature portion of this invention, and the one example is shown in drawing 2. They are PD and PU, a dead zone being set up in these filter circuits 4a and 4b. Phase contrast signals RU and RD with which pulse width (phase contrast information is included) does not change It is generated.

[0025] These phase contrast signals RU and RD It becomes the control voltage of VCO7 by being inputted into a loop filter 6 and finding the integral through the charge pump 5.

[0026] The output of this VCO7 serves as local oscillation frequency in a receiving system, change instructions of a receiving channel are answered, the oscillation frequency fR of reference frequency VCO 1 and the division ratio of the program divider 2 are controlled, and the PLL frequency synthesizer is constituted.

[0027] Drawing 2 (A) and (B) are each example circuit diagram of the filter circuits 4a and 4b of drawing 1. First, if drawing 2 (A) is referred to, it is the lead signal PU. It is inputted into delay circuit 11a and time constant circuit 10a, respectively. The delay output of delay circuit 11a turns into a clocked into of D-FF13a which constitutes latch circuit 12a. [0028] The output of time constant circuit 10a turns into a base input of PNP transistor 15a which constitutes latch circuit 12a, and the emitter output of this transistor 15a turns into one input of OR-gate 14a while turning into a data input of D-FF13a. The delay output of delay circuit 11a is impressed to the other inputs of this OR-gate 14a, or the output is the reset input of D-FF13a. And the reversal Q output of D-FF13a is RU. It becomes.

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[0030] Drawing 3 is each signal wave form view showing operation of the circuit of drawing 2 (B), and is fR. fP When it receives and a phase is overdue, it is the delay signal PD. Two PDs from which it is a thing at the time of being outputted, and it is behind in this example, and a degree differs The pulse is shown.

[0031] PD shown in (C) A pulse is changed into the loose wave (integration wave) of the standup shown in (d) with the time constant of time constant circuit 10b. This wave is the threshold Vt of transistor 15b. PD which is not attained By the pulse, transistor 15b does not turn on and, therefore, the data input signal (D input signal) from inverter 16b to D-FF13b is not generated. On the other hand, an integration wave is Threshold Vt. PD to attain By the pulse, transistor 15b is generated, as it turns on and a data input signal shows (e) from inverter 16b, and for this data input signal, an integration wave is Threshold Vt. It is generated until it becomes smallness.

[0032] the clocked into of D-FF13b -- PD a pulse -- time tD only -- **** delay PD shown in delayed (f) The pulse is supplied. Here, it is a time delay tD. Same [in the time tM (refer to drawing (e)) to become settled with the time constant of time constant circuit 10b / almost] or it is tM. tD If it selects to smallness a little, it synchronizes with the standup timing of a clock signal (delay pulse PD), and a data input signal is incorporated and latched to D-FF13b.

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[0034] Therefore, lead signal PD according to phase contrast Therefore, it is the threshold Vt of filter circuit 12b, without being inputted into the latter charge pump 5 by letting filter circuit 4b (drawing 1) pass depending on the degree of the phase contrast. Time tM to become settled It becomes a dead zone.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram of the PLL circuit by this invention.

[Drawing 2] It is the circuit diagram showing an example of the filter circuits 4a and 4b of drawing 1.

[Drawing 3] It is each part operation wave form chart of the circuit of drawing 2.

[Drawing 4] It is the phase-comparison property view of the PLL circuit by this invention.

[Drawing 5] It is the circuit diagram of the phase comparator of the conventional PLL circuit.

[Drawing 6] It is each wave form chart of the circuit of drawing 5 of operation.

[Drawing 7] It is each wave form chart of the circuit of drawing 5 of operation.

[Drawing 8] It is the phase-comparison property view of the circuit of drawing 5.

[Description of Notations]

1 Reference Frequency VCO

2 Counting-down Circuit

3 Phase Comparator

4a, 4b Filter circuit

5 Charge Pump

6 Loop Filter

7 VCO

10a, 10b Time constant circuit

11a, 11b Delay circuit

12a, 12b Latch circuit

13a, 13b D-FF

14a, 14b OR gate

15a, 15b Transistor

16b Inverter

[Translation done.]

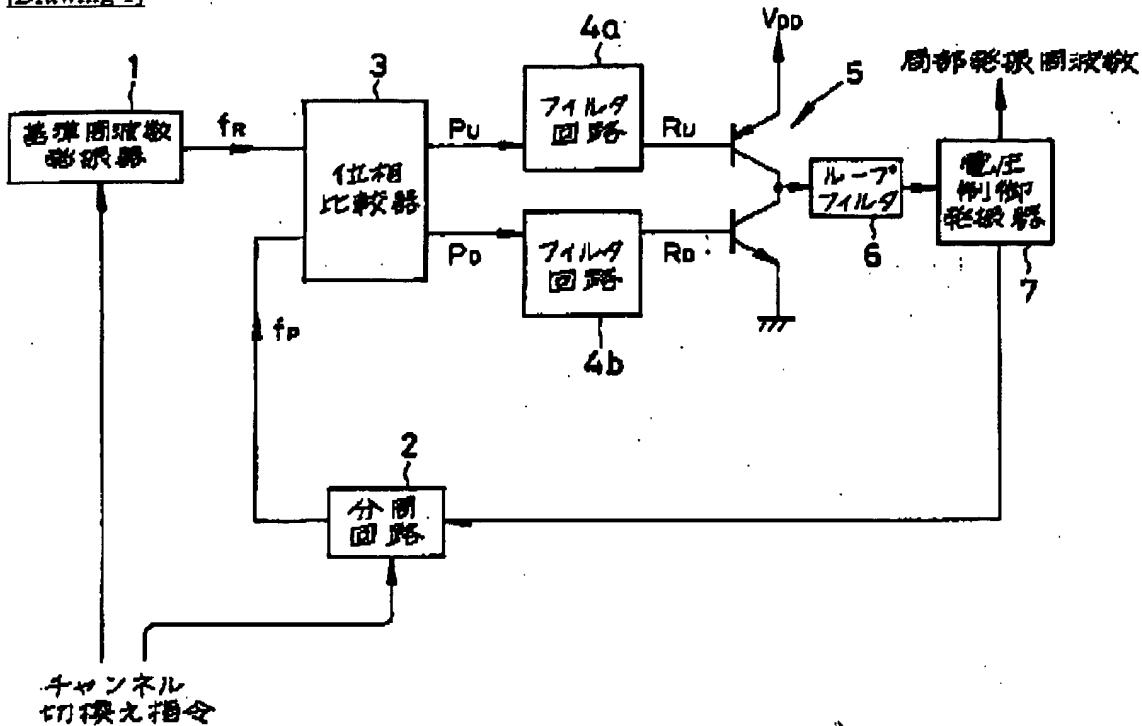
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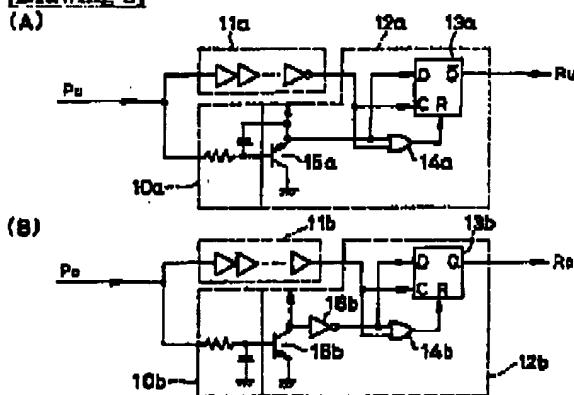
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DRAWINGS

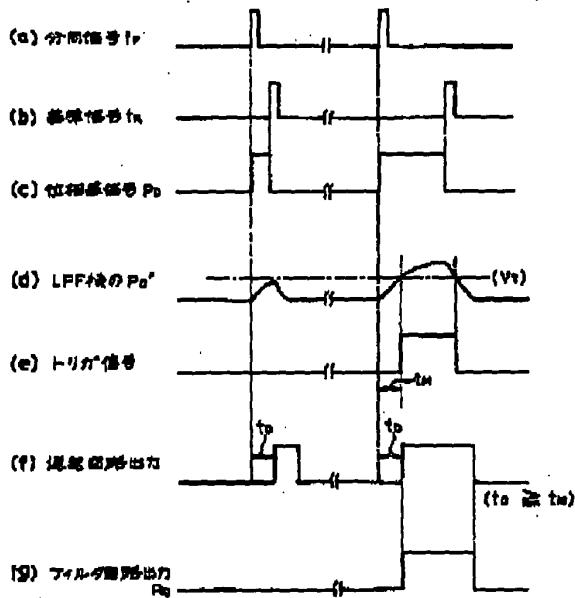
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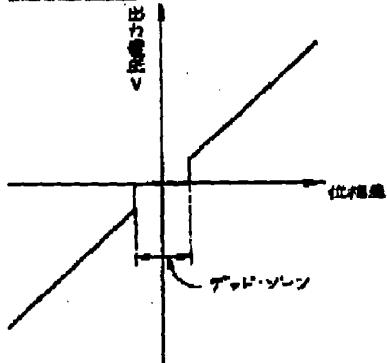
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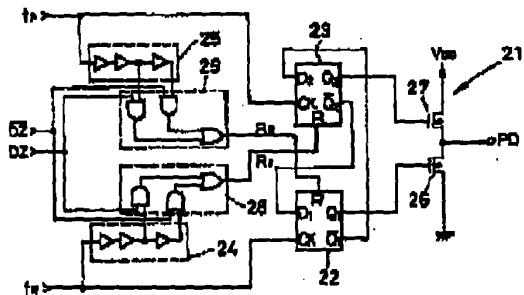
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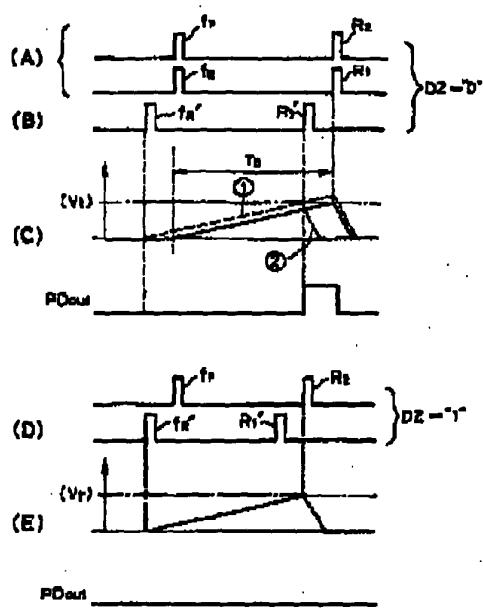
[Drawing 4]



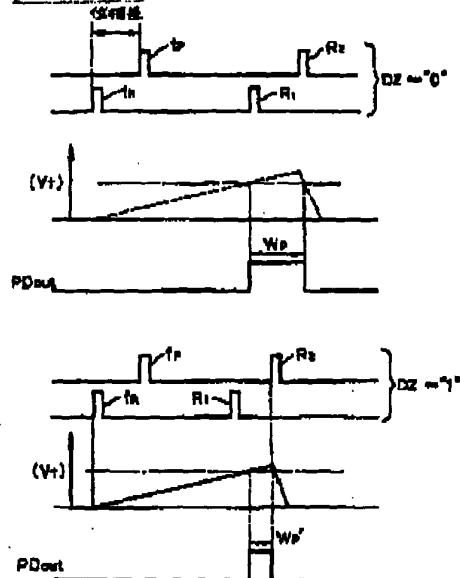
[Drawing 5]



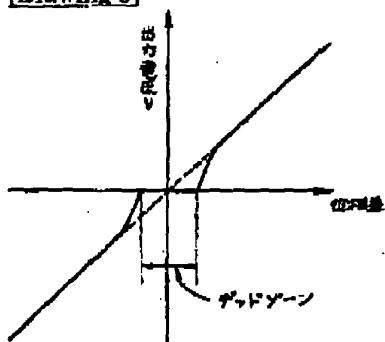
[Drawing 6]



[Drawing 7]



[Drawing 8]



[Translation done.]